PATENT

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Examiner: Richard Ellis

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Applicant(s): John S. Yates, Jr., et al.

Title: COMPUTER WITH TWO EXECUTION MODES

I certify that this correspondence, along with any documents referred to therein, is being transmitted by facsimile on December 2, 2002 to The Commissioner for Patents, Box AF, Washington D.C. 20231.

David E. Boyle

COMMISSIONER FOR PATENTS
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Do Not Enter
RCE 2/6/2002

RESPONSE TO OFFICE ACTION OF OCTOBER 1, 2002

Kindly amend the application as follows.

In the claims:

1. (twice amended) A computer, comprising:

a processor pipeline designed to alternately execute instructions coded for first and second different computer architectures or coded to implement first and second different processing conventions;

a memory for storing instructions for execution by the processor pipeline, the memory being divided into pages for management by a virtual memory manager, a single address space of the memory having first and second pages;

a memory unit designed to fetch instructions from the memory for execution by the pipeline, and to fetch stored indicator elements associated with respective memory pages of the single address space from which the instructions are to be fetched, each indicator element designed to store an indication of which of two different computer architectures and/or execution conventions under which instruction data of the associated page are to be executed